Assiut University
Faculty of Engineering

EE0513-ELECTRONIC CIRCUITS
First Term Final Exam
January 2017

Mechatronics Program

Attempt all questions, full mark: 40 Points **Time: 3 Hours**

Question #1: (10 Points)

Mark True (✓) or False (x)

X	1)	Voltage-divider bias is rarely used.
X	2)	*h*-parameters are never specified on a datasheet.
✓	3)	In a ***CE*** amplifier, the gain can be stabilized by using a swamping resistor.
✓	4)	A differential amplifier amplifies the difference of two input signals.
X	5)	A ***CB*** amplifier has high current gain.
X	6)	When a transistor is saturated, the collector current is minimum.
✓	7)	In an amplifier, a coupling capacitor should appear ideally as a short to the signal.
✓	8)	Class ***AB*** operation overcomes the problem of crossover distortion.
✓	9)	Darlington transistors can be used to increase the input resistance of a class ***AB*** amplifier.
✓	10)	The ***JFET*** always operates with a reverse-biased gate-to-source *pn* junction.
X	11)	The drain current I_D of a ***JFET*** becomes zero if V_{DS} is at the pinch-off voltage.
X	12)	Forward transconductance is the change in drain voltage for a given change in gate voltage.
✓	13)	A ***D-MOSFET*** has a physical channel and an ***E-MOSFET*** has an induced channel.
✓	14)	An analog switch is controlled by a digital input.
X	15)	If the feedback resistor in an inverting amplifier opens, the gain becomes zero.
X	16)	The gain of a voltage-follower is very high.
X	17)	An ideal op-amp has very high output impedance.
✓	18)	An ***R/2R*** ladder circuit is one form of Digital to Analog Converter.
✓	19)	Negative feedback reduces the gain of an op-amp from its open-loop value.
X	20)	When a triangular waveform is applied to a differentiator, a sine wave appears on the output.

Question #2: (6 Points)
Choose the right answer:

1) A transistor circuit has V_{CC} = 12 V, V_{BB} = 3 V, R_C = 2 KΩ, R_B = 50 KΩ, and β_{DC} = 80, the transistor is

C

(A) being driven into saturation (B) being driven into cutoff
(C) being driven in the active region (D) operating nonlinearly

2) The voltage gain of a common-base amplifier is

C

(A) very low (B) very high
(C) the same as a CE (D) the same as a CC

3) The main advantage of a common-collector amplifier is

C

(A) high current gain (B) high voltage gain
(C) high input impedance (D) low input impedance

4) The main advantage of the class-B amplifier over the class-A one is

D

(A) higher current gain (B) higher voltage gain
(C) higher power gain (D) higher efficiency

5) The efficiency of a power amplifier is the ratio of the power delivered to the load to

C

(A) the input signal power (B) the power dissipated in the last stage
(C) the power from the dc power supply (D) none of these answers

6) The maximum efficiency of a class A power amplifier is

A

(A) 25% (B) 50%
(C) 75% (D) 78.5%

7) In a JFET, I_{DSS} is

C

(A) the drain current with the source shorted (B) the drain current at cutoff
(C) the maximum possible drain current (D) the midpoint drain current

8) The drain current in a JFET is controlled by

A

(A) the gate-to-source voltage (B) the drain-to-source voltage
(C) the gate-to-drain voltage (D) the gate current

9) For a p-channel JFET, drain current in the constant-current region increases when

A

(A) the gate-to-source bias voltage decreases (B) the gate-to-source bias voltage increases
(C) the drain-to-source voltage increases (D) the drain-to-source voltage decreases

10) The op-amp common-mode gain is

B

(A) very high (B) very low
(C) always unity (D) unpredictable

11) In a zero-level detector, the output changes state when the input

C

(A) is positive (B) is negative
(C) crosses zero (D) has a zero rate of change

12) In a scaling adder, the input resistors are

C

(A) all the same value (B) all of different values
(C) each proportional to the weight of its input (D) related by a factor of two

Question #3: (10 Points)

a) A certain transistor has α_{DC}= 0.99. If the dc base current is 10 µA, determine r_e'.

r_e' = 25 Ω

b) An n-channel JFET has I_{DSS} = 5 mA and $V_{GS(off)}$ = -8 V. What value of V_{GS} is required to set up a drain current of 2.25 mA.

V_{gs} = -2.63 V

c) A certain class A power amplifier has V_{CEQ}= 12 V and I_{CQ}= 1A. Find the maximum signal power output.

$P_{L(max)}$ = 6 W

d) What bias voltage is developed at the base of a transistor if both resistors in a voltage divider are equal and V_{CC}=10V?

V_B = 5 V

e) An n-channel JFET with voltage-divider bias has a gate voltage of 3V, a drain current of 9 mA, and a source resistance of 800 Ω. Calculate V_{GS}.

V_{gs} = -4.2 V

f) What is the major difference in construction of the D-MOSFET and the E-MOSFET?

A *D-MOSFET* has a physical channel; while an *E-MOSFET* has an induced channel.

g) A common-emitter amplifier is driving a load resistance R_L= 10 kΩ. If R_C = 2.2 kΩ, I_{CQ} = 2.5mA, β_{ac} = 75 and R_E is completely bypassed at the operating frequency. Find the voltage gain.

A_v = -180

h) If the gate-to-source voltage in an n-channel D-MOSFET is made more negative, what would be the effect on the drain current?

Decreases.

i) What is the major difference in construction of the MOSFET and the JFET?

In *MOSFET*, the gate is isolated from the channel by SiO_2 layer; while in the *JFET*, the gate constructs a reverse biased *pn*-junction with the channel.

j) What is the feedback element in an ideal op-amp integrator?

A capacitance.

Question #4: (5 Points)

The silicon ***npn*** transistors used in the two-stage amplifier shown in Fig.4 has $\beta_{dc} = \beta_{ac} = 100$.

a) Find the operating point and r_e' for each transistor. (2 Points)
b) Find the voltage gain and input impedance of each stage. (2 Points)
c) Find the overall voltage gain and input impedance of the amplifier. (1 Point)

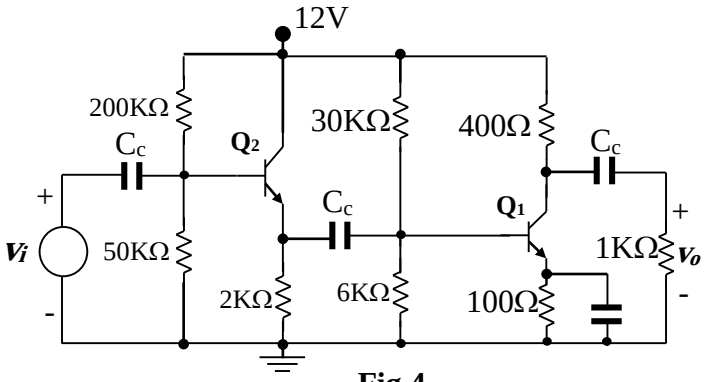

Fig.4

I_{CQ1} = 8.67 mA	V_{CEQ1} = 8.53 V	$r_e'_1$ = 2.88 Ω
I_{CQ2} = 0.71 mA	V_{CEQ2} = 10.58 V	$r_e'_2$ = 35.3 Ω
A_{v1} = -99.2	Z_{in1} = 272 Ω	
A_{v2} = 1	Z_{in2} = 16.3 KΩ	
A_{vT} = -99.2	Z_{inT} = 16.3 KΩ	

Question #5 (2 Points)

The class ***AB*** amplifier in Fig.5 is operating with a single power supply.

a) Assuming the input peak-to-peak voltage is 10 V; determine the power delivered to the load resistor and the amplifier efficiency. (1 Point)
b) What is the maximum power that could be delivered to the load resistor? (1/2 Point)
c) Assume the power supply voltage is raised to 30 V. What is the new maximum power that could be delivered to the load resistor? (1/2 Point)

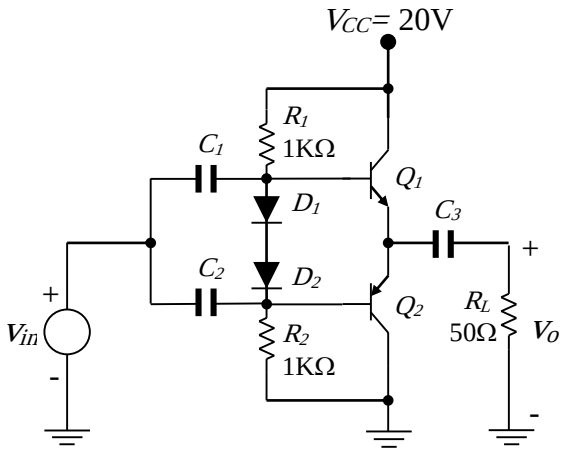

Fig.5

a) P_{LD} = **0.25 W** Efficiency = **39.3 %**

b) $P_{LD(max)}$ = **1 W**

c) $P_{LD(max)}$ = **2.25 W**

Question #6: (3 Points)

The E-MOSFET used in the common-source amplifier in Fig.6 has $I_{D(on)}$ = 135 mA at V_{GS} = 4 V and $V_{GS(th)}$ = 2.5 V.

a) Determine the operating point V_{GSQ}, I_{DQ} and V_{DSQ}.
b) Calculate the value of the transconductance g_m at the Q-point.
c) Determine the voltage gain and input impedance of the amplifier.

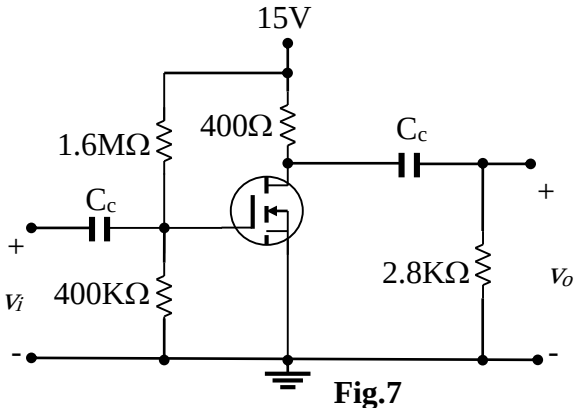

Fig.7

V_{GSQ}= 3 V	I_{DQ}= 15 mA	V_{DSQ} = 9 V
g_m= 60 mS	A_v= -21	Z_{in}= 320 KΩ

Question #7: (2 Points)

a) Find the output voltage when the indicated input voltages are applied to the scaling adder of Fig.7. (1 Point)
b) What is the value of the current through R_f? (1 Point)

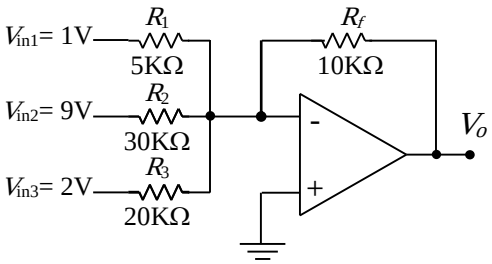

Fig.7

V_o= -6 V	I_f = 0.6 mA

Question #8: (2 Points)

The voltage waveform of Fig.8a is applied to the non-inverting amplifier of Fig.8b. Sketch the output waveform v_o.

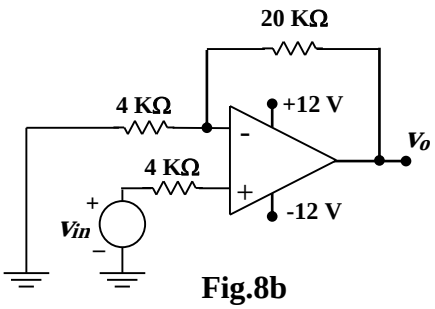

Fig.8b

Fig.8a